R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

IN THE DRAWINGS

The objection to the drawings is traversed. FIG. 2 illustrates an example of a functional portion (the FPGA core 116) and a logic portion (the combinational logic 130). Claim 2 has been amended to clarify Applicants' position. Furthermore, while Applicants' representative does not necessarily agree with the Examiner's position regarding the "internal state machine," the language has been removed from the claims. Therefore, the objection to the drawings should be withdrawn.

CLAIM OBJECTIONS

The objection to claims 1, 10 and 21 under 35 U.S.C. §112 has been obviated, in part, by appropriate amendment and traversed, in part, should be withdrawn. In particular:

Claim 2 has been clarified by adding punctuation.

Claim 22 has been amended.

Claims 26 and 28 have support on page 15 of the specification.

Claim 32 has been amended.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of (i) claims 1, 4-9 and 11-33 under 35 U.S.C. §102(e) as being anticipated by Killian '683 has been obviated by appropriate amendment and should be withdrawn.

Claim 1 provides a system for designing an integrated circuit (IC). The system generally comprises a functional portion, a logic portion, a debugging/fix circuit and a diagnostic architecture. The logic portion generally includes one or more interfaces. The programmable portion may be configured to detect, correct and diagnose errors in the logic portion through the one or more interfaces. The debugging/bug fix circuit may be configured to detect errors in the logic portion. The diagnostic architecture may use the FPGA core in a system on a chip design.

Killian does not disclose or suggest each and every element of the presently claimed invention. In particular, Killian does not appear to disclose or suggest a diagnostic architecture, as presently claimed. For example, the logic portion of the presently claimed invention is configured to (a) detect errors, (b) fix errors, and (c) verify fixes of errors. While Killian discusses detecting errors in the text of the figures cited by the Examiner, Killian appears silent regarding fixing errors. A word search of the word "fix" is consistent with this interpretation. A single occurrence appears in the background of Killian (see column 2, line 40). However, this passage merely refers to

programmability, similar to the claimed functional portion. Killian is silent concerning the claimed logic portion configured to detect and fix errors in the claimed functional portion. Clarification is requested. As such, claim 1 of the present invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 26 of the present invention provides a method for diagnostics comprising the steps of (A) interfacing a chip with an FPGA core, (B) presenting one or more internal signals of the chip, (C) verifying and fixing bugs in the chip with one or more internal signals and (D) programming the FPGA core to dump data from a host register every N clock cycles. Killian is silent regarding at least the step of processing the FPGA core to dump data from a host register every N clock cycles. The citations provided do not appear to address the N clock cycles limitation. Clarification is requested. As such, claim 26 is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-24 and 26 depend, directly or indirectly from the independent claims, which are now believed to be allowable.

COMPLETENESS OF THE OFFICE ACTION

Aside from a notice of allowance, Applicant's representative respectfully requests any further action on the

merits be presented as a non-final action. 37 CFR §1.104(b) states:

> (b) *Completeness of examiner's action.* The examiner's **action will be complete as to all matters**, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

It is unclear what all of the rejections to the claims are. In particular, page 2 of the Office Action states that the previous rejections have been repeated and retained. However, the previous rejections were not repeated, and do not appear particularly relevant in view of the previous amendments. Since the Examiner regrettably failed to return a phone message intended to clarify this issue, Applicants' representative interprets only the portions of the previous rejections actually repeated to be pending.

Furthermore, the Office Action includes several omnibus rejections that simply list most of the claim elements and then assert that the claim elements are disclosed somewhere among one or more figures and/or dozens of text lines contrary to MPEP §707.07(d). For example, the mere parenthetical reference to FIGS. 1-3 and 5-15 as reading on a functional portion configured to detect, fix and verify errors in the functional portion (see page 3 of the Office Action) is less than complete. As such, the Office

Action mailed November 4, 2003 is incomplete and should be withdrawn as an action on the merits.

Furthermore, the amendments to the claims contain either (i) subject matter from one or more previously pending claims, (ii) clarification, or (iii) minor corrections to address objections. As such, the amendments do not raise any new issues and should be entered for purposes of appeal.

As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

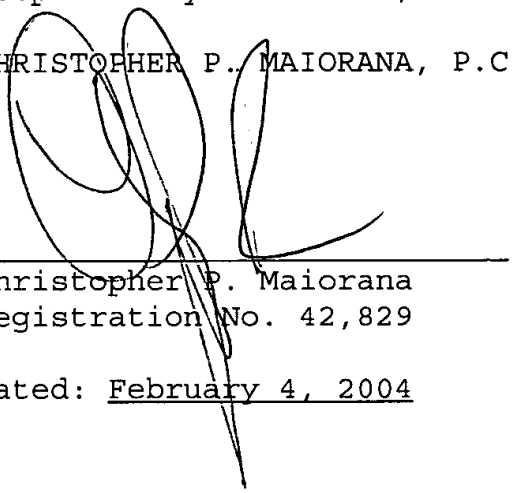
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Christopher P. Maiorana
Registration No. 42,829

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c/o Leo Peters
LSI Logic Corporation
1621 Barber Lane, MS D-106 Legal
Milpitas, CA 95035
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